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EXAMINER	
HAILE, FEBEN	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,439	CHOI, SANG JUN	
	Examiner	Art Unit	
	Feben M. Haile	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12,14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-12, 14, 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In view of applicant's amendment filed October 04, 2006, the application is still in prosecution with respect to claims 1-28.

2. The Applicant has cancelled claims 5, 13, 15 and 27-28, thus only claims 1-4, 6-12, 14, and 16-26 are still pending.

3. The Applicant has failed to file a terminal disclaimer for overcoming the double patenting rejection, thus the rejection still stands

4. The amendment filed is insufficient to overcome the rejection of claims 1-14, 16-26, based upon Dempo (US 6,594,267) as set forth in the previous Office action.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-28 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Pub No. 2002/0080788, hereinafter referred to as Cheon Lee. Although the conflicting claims are not identical, they are variations of each other that are not patentably distinct.

Regarding claim 1, Cheon Lee discloses a) dividing an input ATM adaptation layer 2 (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(claim 1; a plurality of receiver circuits for demultiplexing an AAL2 packet for converting into at least one CPS packet)**; b) sequentially storing the divided CPS packets into first storage areas and sequentially storing first identifiers of the first storage areas **(claim 1; a plurality of memories that store at least one CPS packet; claim 2; a first table for managing VPVC/CID and routing information)**; c) reading the stored first identifiers, sequentially storing the read CPS packets in second storage areas used to route the CPS packets to each destination, and sequentially storing second identifiers of the second storage areas **(claim 1; searching the plurality of memories; claim 2; a second table for managing VPVC/CID information of the searched packets)**; and d) reading the CPS packets, in the order of the second identifiers, from the second storage areas and multiplexing the read CPS packets to generate a reconstructed AAL2 cell

(claim 1; a plurality of transmitter circuits search the plurality of memories and convert the CPS packet into an AAL2 packet by multiplexing).

Regarding claim 14, Cheon Lee discloses a reassembly processing unit that divides an input-ATM adaptation layer (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(claim 1; a plurality of receiver circuits for demultiplexing an AAL2 packet for converting into at least one CPS packet)**; a first memory that sequentially stores the divided CPS packets into first storage areas and sequentially stores first identifiers of the first storage areas **(claim 1; a plurality of memories that store at least one CPS packet; claim 2; a first table for managing VPVC/CID and routing information)**; a CPS packet switching unit that reads the stored CPS packets from the first storage areas in the order of the stored first identifiers and routes the read CPS packets to each destination **(claim 1; searching the plurality of memories; claim 2; a second table for managing VPVC/CID information of the searched packets)**, a second memory that sequentially stores the routed CPS packets into second storage areas and sequentially stores second identifiers of the second storage areas **(claim 1; searching the plurality of memories; claim 2; a second table for managing VPVC/CID information of the searched packets)**; and an assembly processing unit that reads the CPS packets from the second storage areas in the order of the second identifiers and multiplexes the CPS packets read from the second storage areas to generate a reconstructed AAL2 cell **(claim 1; a plurality of transmitter circuits search the plurality of memories and convert the CPS packet into an AAL2 packet by multiplexing)**, wherein the CPS packet switching unit changes origination channel

identifiers (CIDs) of the CPS packets read from the first storage areas to corresponding destination CIDs and sequentially stores the read CPS packets in the second storage areas corresponding to the destination CIDs **(claim 2; a first table for managing VPVC/CID of packets and a second table for managing VPVC/CID information of the searched packets; claim 12; generating new CID for searched packets)**.

Regarding claim 16, Cheon Lee discloses first, second, third, and fourth memories that sequentially store ATM adaptation layer 2 (AAL2) type common part sublayer (CPS) packets and output the CPS packets in order of their respective storage, wherein each memory has storage areas **(claim 1; a plurality of memories that store at least one CPS packet; claim 5; each of the memories is divided into storage areas that correspond to a plurality of output ports)**; a reassembly processing unit that divides an input AAL2 cell into the AAL2 type CPS packets, stores the divided CPS packets in different first storage areas of the first memory in accordance with corresponding virtual paths/virtual channels (VPs/VCs), and stores first identifiers of the different first storage areas in the second memory **(claim 1; a plurality of receiver circuits for demultiplexing an AAL2 packet for converting into at least one CPS packet and a plurality of memories that store at least one CPS packet; claim 2; a first table for managing VPVC/CID and routing information and a second table for managing VPVC/CID information of searched packets)**; a CPS packet switching unit that reads the CPS packets stored in the first memory in the order of the first identifiers stored in the second memory, stores the read CPS packets in different second storage areas of the third memory in accordance with corresponding destination channel

identifiers (CIDs), and stores second identifiers of the second storage areas in the fourth memory **(claim 1; a plurality of memories that store at least one CPS packet & searching the plurality of memories; claim 2; a first table for managing VPVC/CID and a second table for managing VPVC/CID information of the searched packets)**; and an assembly processing unit that reads the CPS packets stored in the third memory in the order of the second identifiers stored in the fourth memory and multiplexes the read CPS packets to generate a reconstructed AAL2 cell **(claim 1; a plurality of transmitter circuits search the plurality of memories and convert the CPS packet into an AAL2 packet by multiplexing)**.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-12, 14, and 16-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Dempo (US 6,594,267), hereinafter referred to as Dempo.

Regarding claim 1, Dempo discloses a) dividing an input ATM adaptation layer 2 (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(figure 4; column 8 lines 4-5; a selector 11 extracts CPS-PDUs from ATM cells)**; b) sequentially storing

the divided CPS packets into first storage areas in accordance with corresponding virtual paths/virtual channels (VPs/VCs) of the respective CPS packets and sequentially storing first identifiers of the first storage areas **(figure 4; column 8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and figures 4-5; column 8 lines 4-10; addresses #1 concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address #1 corresponds to VPI & VCI)**; c) reading the stored first identifiers, sequentially storing the read CPS packets in second storage areas used to route the CPS packets to each destination, and sequentially storing second identifiers of the second storage areas in accordance with respective destination channel identifiers **(figure 4; column 8 lines 11-13 & 23-31; a processing section 17 extracts CPS packets from the CPS-PDUs stored in the FIFO memory 12 and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address concerning each of the CPS packets are stored in FIFO memory 19 and figures 4-5; column 8 lines 23-31; a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address #2 corresponds to an output CID)**; and d) reading the CPS packets, in the order of the second identifiers, from the second storage areas and multiplexing the read CPS packets to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an**

ATM cell), wherein c) further comprises changing origination CIDs of the read CPS packets to corresponding destination CIDs, and sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs **(figures 4-5; column 20 lines 5-27; the processing section 17 alters input CID information to output CID information and figures 4-5; column 8 lines 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID)**.

Dempo fails to explicitly teach the manner of the FIFO operation.

However, one of ordinary skill in the art at the time the invention was made is familiar with a sequential mode of storing data in accordance with any type of information, i.e. iad2, LI, VPI, VCI, or CID.

Regarding claim 2, Dempo discloses changing origination channel identifiers (CIDs) of the read CPS packets to corresponding destination CIDs **(figures 4-5; column 20 lines 5-27; the processing section 17 alters input CID information to output CID information)**; and sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs **(figures 4-5; column 8 lines 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID)**.

Regarding claim 3, Dempo discloses wherein the CPS packets are stored in the first and second storage areas according to their respective order of arrival **(figure 4;**

column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and the FIFO memory 18 stores CPS packets outputted by the processing section 17; one of ordinary skill in the art recognizes the well known practice of positioning packets in storage units by the order of their arrival).

Regarding claim 4, Dempo discloses wherein the CPS packets are read from the first and second storage areas according to their respective order of storage **(one of ordinary skill in the art recognizes the well known practice of transmitting packets from storage units by the order of their arrival).**

Regarding claim 6, Dempo discloses generating a first reference table that maps each of the first identifiers within the corresponding virtual path/virtual channel (VP/VC) **(figure 5; column 18 lines 55-58; a path setting table maps addresses #1 with input VPIs and VCIs)**; and generating a second reference table that maps each of the second identifiers with the corresponding channel identifier (CID) **(figure 5; column 18 lines 55-58; a path setting table maps addresses #2 with output CIDs).**

Regarding claim 7, Dempo discloses wherein the first and second identifiers are stored in the order that the CPS packets ate stored to the corresponding first and second storage areas, respectively **(figures 4-5; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in the FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address has corresponding VPI, VCI, & CID information and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2**

concerning each of the CPS packets are stored in FIFO memory 19; where each address has corresponding VPI, VCI, & CID information).

Regarding claim 8, Dempo discloses wherein the CPS packets are read from the first and second storage areas according to their respective order of storage **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and the FIFO memory 18 stores CPS packets outputted by the processing section 17; one of ordinary skill in the art recognizes the well known practice of positioning packets in storage units by the order of their arrival and transmitting the packets from the storage units by the order of their arrival).**

Regarding claim 9, Dempo discloses implementing a switching test by reading the CPS packets from the second storage areas in the order of the second identifiers and comparing the read CPS packets to a standard **(figure 4; column 11 lines 6-23; a CPS-PDU processing section reads out a CPS packet from a memory according to its corresponding address and also executes a parity check; one of ordinary skill in the art recognizes that error detection can be performed using header error control, which is an IEEE 802.11b standard).**

Regarding claim 10, Dempo discloses implementing a switch signaling by reading the CPS packets from the second storage areas in the order of the second identifiers and outputting the read CPS packets to a processor **(figure 4; column 8 lines 5-10 & 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17; one of ordinary skill in the art recognizes the well known**

practice of positioning packets in storage units by the order of their arrival and transmitting the packets from the storage units by the order of their arrival; one of ordinary skill in the art recognizes the well known practice of positioning packets in storage units by the order of their arrival and transmitting the packets from the storage units by the order of their arrival).

Regarding claim 11, Dempo discloses routing the CPS packets stored in the first storage areas to another switch in the order of the first identifiers **(figure 4; column 8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12; one of ordinary skill in the art recognizes the well known practice of positioning packets in storage units by the order of their arrival and transmitting packets from the storage units by the order of their arrival).**

Regarding claim 12, Dempo discloses wherein the first and second storage areas have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).**

Regarding claim 14, Dempo discloses a reassembly processing unit that divides an input-ATM adaptation layer (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(figure 4; column 8 lines 4-5; a selector 11 extracts CPS-PDUs from ATM cells)**; a first memory that sequentially stores the divided CPS packets into first storage areas and sequentially stores first identifiers of the first storage areas **(figure 4; column**

8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13); a CPS packet switching unit that reads the stored CPS packets from the first storage areas in the order of the stored first identifiers and routes the read CPS packets to each destination **(figure 4; column 8 lines 11-13; a processing section 17 extracts CPS packets from the CPS-PDUs stored in the FIFO memory 12)**, a second memory that sequentially stores the routed CPS packets into second storage areas and sequentially stores second identifiers of the second storage areas **(figure 4; column 8 lines 23-31; a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19)**; and an assembly processing unit that reads the CPS packets from the second storage areas in the order of the second identifiers and multiplexes the CPS packets read from the second storage areas to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an ATM cell)**, wherein the CPS packet switching unit changes origination channel identifiers (CIDs) of the CPS packets read from the first storage areas to corresponding destination CIDs and sequentially stores the read CPS packets in the second storage areas corresponding to the destination CIDs **(figures 4-5; column 20 lines 5-27 & column 8 lines 23-31; the processing section 17 alters input CID information to output CID information and the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address**

concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID).

Dempo fails to explicitly teach the manner of the FIFO operation.

However, one of ordinary skill in the art at the time the invention was made is familiar with a sequential mode of storing data in accordance with any type of information, i.e. iad2, LI, VPI, VCI, or CID, is obvious to one of ordinary skill in the art.

Regarding claim 16, Dempo discloses first, second, third, and fourth memories that sequentially store ATM adaptation layer 2 (AAL2) type common part sublayer (CPS) packets and output the CPS packets in order of their respective storage, wherein each memory has storage areas **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19)**; a reassembly processing unit that divides an input AAL2 cell into the AAL2 type CPS packets, stores the divided CPS packets in different first storage areas of the first memory in accordance with corresponding virtual paths/virtual channels (VPs/VCs), and stores first identifiers of the different first storage areas in the second memory **(figures 4-5; column 8 lines 4-10; a selector 11 extracts CPS-PDUs from ATM cells and the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses #1 concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address corresponds to a VPI & VCI)**; a CPS packet switching unit that reads the CPS packets stored in the first memory in the order of the first identifiers

stored in the second memory, stores the read CPS packets in different second storage areas of the third memory in accordance with corresponding destination channel identifiers (CIDs), and stores second identifiers of the second storage areas in the fourth memory **(figures 4-5; column 8 lines 23-31; a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an output CID)**; and an assembly processing unit that reads the CPS packets stored in the third memory in the order of the second identifiers stored in the fourth memory and multiplexes the read CPS packets to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an ATM cell)**.

Dempo fails to explicitly teach the manner of the FIFO operation. However, one of ordinary skill in the art at the time the invention was made is familiar with a sequential mode of storing data in accordance with any type of information, i.e. iad2, LI, VPI, VCI, or CID, is obvious to one of ordinary skill in the art.

Regarding claim 17, Dempo discloses a first reference table that maps the first identifiers with the corresponding VPs/VCs **(figure 5; column 18 lines 55-58; a path setting table maps addresses #1 with input VPIs and VCIs)**; and a second reference table that maps the second identifiers with the corresponding destination CIDs **(figure 5; column 18 lines 55-58; a path setting table maps addresses #2 with output CIDs)**.

Regarding claim 18, Dempo discloses wherein the reassembly processing unit refers to the first reference table to determine the first storage areas corresponding to the VPS/VCS of the CIDS packets **(figures 4-5; column 8 lines 5-10; the selector 11 receives the addresses concerning the CPS-PDUs and stores them FIFO memory 13, where each address corresponds to a VPI & VCI)**.

Regarding claim 19, Dempo discloses wherein the CPS packet switching unit refers to the second reference table to determine the respective destination CIDs corresponding to the CPS packets **(figures 4-5; column 8 lines 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to a output CID)**.

Regarding claim 20, Dempo discloses wherein the CPS packet switching unit changes origination CIDs of the CPS packets read from the fist memory to the corresponding destination CIDs, with reference to the second reference table **(figures 4-5; column 20 lines 5-27 & column 8 lines 23-31; the processing section 17 alters input CID information to output CID information and the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID)**.

Regarding claim 21, Dempo discloses wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively **(figures 4-5; column 8 lines 5-10 & 23-31; the**

CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address has corresponding VPI, VCI, & CID information and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19; where each address has corresponding VPI, VCI, & CID information).

Regarding claim 22, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).**

Regarding claim 23, Dempo discloses a central processing unit that reads the CIDS packets from the first memory in the order of the stored first identifiers and implements testing and signaling for switching **(figure 4; column 11 lines 6-23; a CPS-PDU processing section reads out a CPS packet from a memory according to its corresponding address and also executes a parity check).**

Regarding claim 24, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18**

stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).

Regarding claim 25, Dempo discloses a plurality of cell switches that each has first, second, third, and fourth memories **(figure 4; FIFO memories 12-13 and 18-19)**, a reassembly processing unit **(figure 4; selector 11)**, a CPS packet switching unit, and an assembly processing unit **(figure 4; packet processing section 17)**; and a router that routes the CPS packets output from one of the plurality of cell switches to another cell switch **(figure 4; multiplexing section 27)**.

Regarding claim 26, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19)**.

Response to Arguments

7. Applicant's arguments filed October 04, 2006 have been fully considered but they are not persuasive.

On page 19, the Applicant acknowledges the double patenting rejection and makes an expressed notion of filing a terminal disclaimer. However the Examiner has not received any such type of documentation, therefore the rejection still stands.

On pages 19-20, the Applicant respectfully traverses that Dempo does not discloses, suggest, or render obvious the limitations in the combination of each of the claims of, inter alia, sequentially storing the read CPS packets in correspondence with the destination CIDs. The Examiner respectfully disagrees with the Applicant. Dempo discloses a FIFO memory 18 receiving CPS packets from a processing section 17 and storing them according to a **FIFO operation (column 14 lines 16-20)**. Dempo further teaches a second FIFO memory 19 receiving, also from the processing section 17, iad2 and LI information concerning each of the CPS packets stored in the FIFO memory 19 and storing them according to a **FIFO operation (column 14 lines 24-28)**. Dempo also suggests that each iad2 has corresponding CID information **(figure 5)**. Although Dempo does not explicitly disclose the manner of the FIFO operation, a sequential mode of storing data in accordance with any type of information, i.e. iad2, LI, VPI, VCI, or CID, is obvious to one of ordinary skill in the art. Therefore as the claims are interpreted in their broadest sense, the Examiner believes that Dempo indeed does render Applicant's invention obvious.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Feben M. Haile whose telephone number is (571) 272-3072. The examiner can normally be reached on 6:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/12/2006

WING CHAN
SUPERVISORY PATENT EXAMINER